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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/078,180	02/19/2002	Neil G. Morrow	TI-31574	5454
23494	7590	11/16/2004	EXAMINER	
TEXAS INSTRUMENTS INCORPORATED P O BOX 655474, M/S 3999 DALLAS, TX 75265			CLEARY, THOMAS J	
			ART UNIT	PAPER NUMBER
			2111	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/078,180

Applicant(s)

MORROW, NEIL G.

Examiner

Thomas J. Cleary

Art Unit

2111

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on 13 August 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 5, 6, and 7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear as to whether the "host bus segment" referred to in Line 3 of Claims 5, 6, and 7 refers to the "first host bus segment" or the "second host bus segment" of Claim 1. It is further unclear as to whether "a serial link" referred to in Lines 6-7 of Claims 5, 6, and 7 refers to the same serial link disclosed in Claim 1.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by the National Semiconductor DS92LV222A Two Channel Bus LVDS MUXed Repeater ("222A Repeater"), as described in the National Semiconductor Datasheet for said DS92LV222A Repeater.

5. In reference to Claim 1, the 222A Repeater discloses a system for extending a signal path of a host bus comprising: a first repeater portion connected to a first segment of the host bus (See 'Connection Diagram' and 'Block Diagram' on Page 1); a second repeater portion connected to a second, non-hierarchical segment of the host bus remote from the first portion of the host bus (See 'Connection Diagram' and 'Block Diagram' on Page 1), where the first and second portions of the repeater are connected by a serial link (See 'Block Diagram' on Page 1).

6. In reference to Claim 2, the 222A Repeater discloses the limitations as applied to Claim 1 above. The 222A Repeater further discloses that the serial link is an LVDS link (See 'General Description' and Bullet 1 of 'Features' on Page 1).

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over the 222A Repeater as applied to Claim 2 above, and further in view of US Patent Application Publication Number 2003/0065869 to Balay et al. ("Balay").

9. In reference to Claim 3, the 222A Repeater teaches the limitations as applied to Claim 2 above. The 222A Repeater does not teach that the host bus is a PCI bus. Balay teaches connecting PCI buses together by converting the PCI signals on the first bus to a high speed serial connection such as LVDS, communicating the signals over the high speed serial connection, and converting the signals back to PCI to be transmitted on the second bus (See Figures 1 and 2 and Page 2 Paragraphs 24-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a 222A Repeater to connect the PCI buses of Balay, resulting in the invention of Claim 3, because PCI is a standard implementation which provides a well-standardized backplane structure that allows different line cards to be connected (See Page 1 Paragraphs 4-5 of Balay).

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over the 222A Repeater as applied to Claim 2 above, and further in view of The Low Pin Count (LPC) Interface Specification from Intel ("Intel 1997").

11. In reference to Claim 4, the 222A Repeater teaches the limitations as applied to Claim 2 above. The 222A Repeater does not teach that the host bus is an LPC (Low Pin Count) bus as defined by Intel 1997. Intel 1997 teaches the use of a serialized LPC bus (See Page 1 Chapter 1 and Page 6 Section 4.2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a 222A Repeater to connect the LPC buses of Intel 1997, resulting in the invention of Claim 4, because LPC has a reduced cost, allows synchronous design, is transparent and thus does not require special drivers or configuration, and supports desktop and mobile implementations (See Page 1 Section 1.1 of Intel 1997).

12. Claims 5, 7, 8, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the 222A Repeater as applied to Claims 1 and 2 above, and further in view of the MoSys Multibank DRAM ("MDRAM") as described by MoSys Preliminary Information Document "MD904 to MD920, ½ to 2½ Mbyte Multibank DRAM (MDRAM) 128Kx32 to 656Kx32."

13. In reference to Claim 5, the 222A Repeater teaches the limitations as applied to Claim 1 above. The 222A Repeater further teaches an interface to the host bus segment (See 'Connection Diagram' and 'Block Diagram' on Page 1) and a link translation layer connected the transaction queue to translate incoming transactions from the host bus into serial streams to be sent over a serial link (See elements 'R0' and

'R1' in 'Block Diagram' on Page 1). The 222A Repeater does not teach a transaction queue with a data buffer connected to the interface. The MDRAM teaches a bus repeater having a FIFO, which is equivalent to a data buffer, connected to the interface (See Figure 1 and Paragraph 2 on Page 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the data buffer of the MDRAM in the 222A Repeater, resulting in the invention of Claim 5, in order to guarantee accurate I/O timing (See Column 1 Paragraph 5 on Page 2 of the MoSys Preliminary Information Document).

14. In reference to Claim 7, the 222A Repeater teaches the limitations as applied to Claim 2 above. The 222A Repeater further teaches an interface to the host bus segment (See 'Connection Diagram' and 'Block Diagram' on Page 1) and a link translation layer connected the transaction queue to translate incoming transactions from the host bus into serial streams to be sent over a serial link (See elements 'R0' and 'R1' in 'Block Diagram' on Page 1). The 222A Repeater does not teach a transaction queue with a data buffer connected to the interface. The MDRAM teaches a bus repeater having a FIFO, which is equivalent to a data buffer, connected to the interface (See Figure 1 and Paragraph 2 on Page 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the data buffer of the MDRAM in the 222A Repeater, resulting in the invention of Claim 7, in order to guarantee accurate I/O timing (See Column 1 Paragraph 5 on Page 2 of the MoSys Preliminary Information Document).

15. In reference to Claim 8, the 222A Repeater and MDRAM teach the limitations as applied to Claim 5 above. The 222A Repeater further teaches a transaction decode circuit connected to the interface to the host bus segment to determine which transactions on the host bus to accept and pass on over the serial link (See elements 'R0' and 'R1' and signal 'RSEL' in 'Block Diagram' on Page 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the data buffer of the MDRAM in the 222A Repeater, resulting in the invention of Claim 8, in order to guarantee accurate I/O timing (See Column 1 Paragraph 5 on Page 2 of the MoSys Preliminary Information Document).

16. In reference to Claim 10, the 222A Repeater and MDRAM teach the limitations as applied to Claim 7 above. The 222A Repeater further teaches a transaction decode circuit connected to the interface to the host bus segment to determine which transactions on the host bus to accept and pass on over the serial link (See elements 'R0' and 'R1' and signal 'RSEL' in 'Block Diagram' on Page 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the data buffer of the MDRAM in the 222A Repeater, resulting in the invention of Claim 10, in order to guarantee accurate I/O timing (See Column 1 Paragraph 5 on Page 2 of the MoSys Preliminary Information Document).



17. Claims 6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over the 222A Repeater as applied to Claim 1 above, and further in view of the MDRAM as described by MoSys Preliminary Information Document "MD904 to MD920, 1/2 to 2 1/2 Mbyte Multibank DRAM (MDRAM) 128Kx32 to 656Kx32."

18. In reference to Claim 6, the 222A Repeater and Balay teach the limitations as applied to Claim 3 above. The 222A Repeater further teaches an interface to the host bus segment (See 'Connection Diagram' and 'Block Diagram' on Page 1) and a link translation layer connected the transaction queue to translate incoming transactions from the host bus into serial streams to be sent over a serial link (See elements 'R0' and 'R1' in 'Block Diagram' on Page 1). The 222A Repeater and Balay do not teach a transaction queue with a data buffer connected to the interface. The MDRAM teaches a bus repeater having a FIFO, which is equivalent to a data buffer, connected to the interface (See Figure 1 and Paragraph 2 on Page 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the data buffer of the MDRAM in the 222A Repeater connecting the PCI buses of Balay, resulting in the invention of Claim 6, in order to guarantee accurate I/O timing (See Column 1 Paragraph 5 on Page 2 of the MoSys Preliminary Information Document).

19. In reference to Claim 9, the 222A Repeater, Balay, and MDRAM teach the limitations as applied to Claim 6 above. The 222A Repeater further teaches a

transaction decode circuit connected to the interface to the host bus segment to determine which transactions on the host bus to accept and pass on over the serial link (See elements 'R0' and 'R1' and signal 'RSEL' in 'Block Diagram' on Page 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the data buffer of the MDRAM in the 222A Repeater, resulting in the invention of Claim 9, in order to guarantee accurate I/O timing (See Column 1 Paragraph 5 on Page 2 of the MoSys Preliminary Information Document).

### ***Response to Arguments***

20. Applicant's arguments filed 13 August 2004 with respect to Claims 1-10 have been fully considered but are moot in view of the new ground(s) of rejection. Applicant has modified the scope of the claims to include the connected bus segments being "non-hierarchical". As shown above, such changes are not persuasive to overcome a rejection based on 35 USC §§ 102 and 103. The new ground(s) of rejection presented in this Office action in reference to the aforementioned claims have been necessitated by the Applicant's amendment.

### ***Conclusion***

21. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: LSI Product Brief "LSI53C120 SCSI HVD Bus Expander"; LSI Product Brief "LSI53C140 SCSI Bus Expander"; National Semiconductor News Release "New Bus LVDS Family Offers Superior Combination of High Speed (155-400 Mbps), Low Power, Low Cost, and Low Noise/EMI"; and Electronicstalk article "Bus repeaters improve signal integrity."

22. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-4), Alt. Fridays (7-3).


If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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